



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/802,417	03/08/2001	Hidekazu Watanabe	80398P348	5418
8791	7590	08/24/2004	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030			LEFKOWITZ, SUMATI	
			ART UNIT	PAPER NUMBER
			2112	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/802,417

Applicant(s)

WATANABE, HIDEKAZU

Examiner

Sumati Lefkowitz

Art Unit

2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 May 2004 and 16 July 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

1. Claims 1-30 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-7, 9-17, 19-27, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jahnke et al., US 2002/0052999 A1 (hereinafter Jahnke) in view of Gehman et al., 6,260,093 (hereinafter Gehman).

As to claims 1-7, 9-17, 19-27, 29, and 30, Jahnke discloses an apparatus (note Figure 3, elements 314, 315, 316) comprising first (note Figure 3, element 314 and circuitry internal to bridge 315 for interfacing with AHB bus) and second (note Figure 3, element 316 and circuitry internal to bridge 315 for interfacing with HTB bus) bus interface circuits to interface to first (note Figure 3, AHB bus 300) and second (note Figure 3, HTB bus 330) buses, respectively, the first bus being accessible to a first processor (note Figure 3, CPU 301), a processor interface circuit (note Figure 3, element 316) to interface to a second master (note Figure 3, element 333), the second master having accessibility to the first and second buses (note Figure 3, element 333, wherein the master 333 has access to the AHB bus 300 and the HTB bus 301 since it can transfer data over both buses), and an arbitration logic circuit (note Figure 3, elements 314 and 316)

Art Unit: 2112

coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first processor and second master, wherein the second master is coupled to the first and second buses (note Figure 3, wherein the second master 333 is coupled to the second bus 330 and the first bus 300 through bridge 315), wherein the processor interface circuit comprises a command decoder to decode an access command from the second processor requesting access to one of the first and second buses (note [0025], wherein the fact that HTB peripheral requests and is granted control of HTB bus implies that a command decoder is present to decode the access request from the peripheral), wherein the arbitration circuit disables the first bus interface circuit when the second processor requests access to the second bus or that the arbitration circuit enables the first and second bus interface circuits when access request to the second bus from the first processor is granted (i.e., inherent in the fact that the bridges allow for independent, concurrent access or isolation of the buses from each other, which would imply that the interfaces, including inherent drivers and receivers, would be disabled to prevent any collisions on the bus, i.e., to insure that only one master has access to each bus at any given time and that the bridges also allow for transactions to cross the bridge, which would imply that the interfaces, including inherent drivers and receivers, would have to be enabled to allow transactions to cross the bridge from one bus to the other), wherein the arbitration logic circuit resolves access requests from the first processor and second master such that the first processor accesses the first bus while the second master accesses the second bus ([0019], wherein the bridge providing isolation between the buses reads on the first processor accessing the first bus while the second master accesses the second bus), wherein the first processor is one of a microprocessor, a micro-controller, and a digital signal processor (note Figure 3, CPU 301),

Art Unit: 2112

wherein the first and second buses are of different types (note AHB bus and HTB bus), further discloses a method comprising interfacing to first (AHB bus) and second buses (HTB bus) by first (note Figure 3, element 314 and circuitry internal to bridge 315 for interfacing with AHB bus) and second (note Figure 3, element 316 and circuitry internal to bridge 315 for interfacing with HTB bus) interface circuits, respectively, the first bus being accessible to a first processor (note Figure 3, CPU 301), interfacing to a second master (note Figure 3, HTB peripheral 333), and arbitrating access requests from the first processor and second master, wherein the second master is coupled to the first and second buses, further discloses a system comprising first (i.e., APB bus) and second (i.e., HTB bus) buses, first processor (note Figure 3, CPU 301) and second master (note Figure 3 HTB peripheral 333), the first processor being coupled to the first bus, a bus controller (note Figure 3, elements 314, 315, and 316) coupled to the first and second buses to control bus access from the first processor and second master, the bus controller comprising first (note Figure 3, element 314 and circuitry internal to bridge 315 for interfacing with AHB bus) and second (note Figure 3, element 316 and circuitry internal to bridge 315 for interfacing with HTB bus) bus interface circuits to interface to the first and second buses, respectively, a processor interface circuit (note Figure 3, element 316) to interface to the second master, and an arbitration logic circuit (note Figure 3, elements 314 and 316) coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first processor and second master (note Figure 3, [0006-0007, 0017-0028]).

Jahnke fails to disclose that the second master is a processor or that the buses are the same buses.

Gehman discloses that the second master is a processor and that the buses are the same buses (note column 3, lines 8-59).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of a processor as the second master so as to allow for the use of intelligent peripherals in the system of Jahnke, as Gehman teaches in column 3, lines 33-36, thereby increasing the functionality of the system of Jahnke.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the buses be the same buses, as Gehman teaches, in the system of Jahnke so as to allow for the addition of more devices, even when existing buses have been loaded to their maximum.

4. Claims 1-7, 11-17, and 21-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crews et al., 5,619,661 (hereinafter Crews) in view of Gehman et al., 6,260,093 (hereinafter Gehman).

As to claims 1-7, 11-17, and 21-27, Crews discloses an apparatus (note Figure 1, bridge chip 30) comprising first (note Figure 1, elements 32, 42, 40) and second (note Figure 1, elements 36, 38, 34) bus interface circuits to interface to first (note Figure 1, primary bus 10) and second (note Figure 1, secondary bus 20) buses, respectively, the first bus being accessible to a first processor (note column 1, lines 9-12), a processor interface circuit (note Figure 1, elements 32, 42, 40) to interface to a second master (note Figure 1, element 18), and an arbitration logic circuit (note Figure 1, elements 32 and 34) coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first processor and second

Art Unit: 2112

master, wherein the arbitration circuit disables the first bus interface circuit when the second processor requests access to the second bus or that the arbitration circuit enables the first and second bus interface circuits when access request to the second bus from the first processor is granted (i.e., inherent in the fact that the bridges allow for independent, concurrent access, which would imply that the interfaces, including inherent drivers and receivers, would be disabled to prevent any collisions on the bus, i.e., to insure that only one master has access to each bus at any given time and that the bridges also allow for transactions to cross the bridge, which would imply that the interfaces, including inherent drivers and receivers, would have to be enabled to allow transactions to cross the bridge from one bus to the other), wherein the second master is coupled to the first and second buses (note Figure 1, wherein the second master 18 is coupled to the second bus 20 and to the first bus 10 through bridge 30), wherein the processor interface circuit comprises a command decoder to decode an access command from the second processor requesting access to one of the first and second buses (note column 5, lines 22-55, wherein the fact that secondary to primary bus transfer requests are granted implies that a command decoder is present to decode the access request from the master on the secondary bus), wherein the arbitration logic circuit resolves access requests from the first processor and second master such that the first processor accesses the first bus while the second master accesses the second bus (note column 3, lines 58 – column 4, line 52), wherein the first processor is one of a microprocessor, a micro-controller, and a digital signal processor (note column 1, lines 9-12), further discloses a method comprising interfacing to first (i.e., primary bus 10) and second (i.e., secondary bus 20) bus by first (note Figure 1, elements 32, 42, 40) and second (note Figure 1, elements 36, 38, 34) interface circuits, respectively, the first bus being accessible to a first

Art Unit: 2112

processor (note column 1, lines 9-12), interfacing to a second master (note Figure 1, master 18), and arbitrating access requests from the first processor and second master, wherein the second master is coupled to the first and second buses, further discloses a system comprising first (i.e., primary bus 10) and second (i.e., secondary bus 20) buses, first processor (note column 1, lines 9-12) and second master (note column 1, master 18), the first processor being coupled to the first bus, a bus controller (note Figure 1, bridge 30) coupled to the first and second buses to control bus access from the first processor and second master, the bus controller comprising first (note Figure 1, elements 32, 42, 40) and second (note Figure 1, elements 36, 38, 34) bus interface circuits to interface to the first and second buses, respectively, a processor interface circuit (note Figure 1, elements 32, 42, 40) to interface to the second master, and an arbitration logic circuit (note Figure 1, elements 32 and 34) coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first processor and second master (note Figure 1 and column 3, line 58 – column 5, line 55).

Crews fails to disclose that the second master is a processor.

Gehman discloses that the second master is a processor (note column 3, lines 8-59).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of a processor as the second master so as to allow for the use of intelligent peripherals in the system of Crews, as Gehman teaches in column 3, lines 33-36, thereby increasing the functionality of the system of Crews.

5. Claims 8, 18, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jahnke et al., US 2002/0052999 A1 (hereinafter Jahnke) in view of Gehman et al., 6,260,093

Art Unit: 2112

(hereinafter Gehman), as applied to claims 1-7, 9-17, 19-27, 29, and 30 above, and further in view of Mergard et al., 5,941,968 (hereinafter Mergard).

As to claims 8, 18, and 28, fails to disclose that the second processor is a DMAC.

Mergard discloses that the second processor is a DMAC (note Figures 1A, 1B, DMA Controller 122).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of a DMAC as the second processor so as to relieve the CPU of the burden of performing memory transfers.

Response to Arguments

6. Applicant's arguments filed on 5/19/04 have been fully considered but they are not persuasive for the following reasons:

Examiner states that arbiters/decoders 314 and 316 together read on Applicant's claimed arbitration logic. Jahnke specifically teaches that these two arbiters are different, indicating that they must be separate. Jahnke teaches away from the claimed invention, which recites an arbitration logic circuit to arbitrate access requests from the first and second processor. Both Jahnke and Gehman do not disclose or suggest an arbitration logic to arbitrate requests from the first and second processors.

Examiner is taking both arbiters/decoders 314 and 316 of Jahnke to be Applicant's arbitration logic circuit. Since Applicant's claims do not recite any language that precludes this interpretation, Examiner believes that the current application of the Jahnke reference to the

Art Unit: 2112

claims is reasonable and correct. In addition, Gehman was not used to teach the claimed arbitration logic. Gehman was used to teach having a second processor as the second master.

Gehman was used to teach the use of a second processor as the second bus master in Jahnke. However, since Gehman does not disclose or suggest a processor interface circuit, Gehman fails to disclose the claimed invention.

Gehman was used to teach a second processor, not the processor interface circuit. Jahnke was used to teach an interface circuit to a second master. Gehman was used to teach having a second processor as the second master so as to allow for the use of intelligent peripherals in the system of Jahnke (Gehman: column 3, lines 33-36) and expanded functionality of Jahnke.

Crews explicitly teaches that the primary arbiter and the secondary arbiter work independently in a concurrent mode of arbitration. Therefore Crews effectively teaches away from the claimed invention because Crews requires two separate arbiters arbitrating requests from the first and second processors separately, not an arbitration logic circuit to arbitrate access requests from both processors, as claimed.

Again, since there is no language in the claims which precludes the interpretation of both the primary and secondary arbiters of Crews as reading on the claimed "arbitration logic circuit...to arbitrate access requests from the first and second processors", it is the examiner's position that this interpretation is reasonable and correct.

The DMAC of Mergard has no access to first and second buses, contrary to the claimed invention.

Mergard was used only to teach the advantage of having the second master of Jahnke be a DMAC, the advantage being relieving the CPU of Jahnke of the burden of carrying out data transfers to and from memory. Jahnke was used to teach a second master having access to first and second buses.

The Examiner failed to present a convincing line of reasoning as to why a combination of Jahnke, Gehman, Crews, and Mergard is an obvious application of the claimed arbitration technique.

Looking at claim 1 and giving the claim language its broadest reasonable interpretation, Jahnke teaches first and second bus interface circuits to interface to first and second buses, the first bus being accessible to a first bus master, which also happens to be a processor, an interface circuit to interface to a second bus master, which does not happen to be a processor, the second bus master having accessibility to the first and second buses, and an arbitration logic circuit to arbitrate access requests from the first and second bus masters. The only things Jahnke does not teach are that the second bus master is a processor or that it is a DMAC. Gehman teaches the advantages of having a processor as the second bus master and Mergard teaches the advantages of having a DMAC as the second bus master. Both Jahnke and Crews, however, teach the underlying, main concept of having an arbitration circuit which acts as bus separator to separate one bus from another so that a bus master on one bus can use its bus while a bus master on the other bus uses its bus, i.e., so that bus masters on both buses can use their respective buses

concurrently. Therefore, given that both Jahnke and Crews teach the main concept of the claimed invention and Gehman and Mergard fill in missing, tangential limitations, the Examiner believes that there is a solid line of reasoning as to why a combination of the references is appropriate.

Examiner has failed to show a teaching, suggestion, or motivation to combine the references.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, taking the combination of Jahnke, Gehman and Mergard, it is the examiner's position that given that Jahnke teaches isolating a bus, coupled to a processor, on one side of a bridge from a bus, coupled to a bus master not disclosed as a second processor, on the other side of the bridge when communication on only one side of the bridge is necessary and not isolating the buses on either side of the bridge when communication across the bridge is necessary, that Gehman teaches having a second processor, and that Mergard teaches that the second processor is a DMAC, one of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings of Jahnke, Gehman and Mergard so as to allow a DMAC and a processor coupled to different buses across a bridge to be isolated from each other when

Art Unit: 2112

communication on only one side of the bridge is necessary or not to be isolated from each other when communication across the bridge is necessary.

With respect to the combination of Crews and Gehman, it the examiner's position that given that Crews teaches isolating a bus, coupled to a processor, on one side of a bridge from a bus, coupled to a bus master not disclosed as a second processor, on the other side of the bridge when communication on only one side of the bridge is necessary and not isolating the buses on either side of the bridge when communication across the bridge is necessary and that Gehman teaches having a second processor, one of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings of Crews and Gehman so as to allow first and second processors coupled to different buses across a bridge to be isolated from each other when communication on only one side of the bridge is necessary or not to be isolated from each other when communication across the bridge is necessary.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sumati Lefkowitz whose telephone number is 703-308-7790. The examiner can normally be reached on Monday-Friday from 6:00-2:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached at 703-305-4815.

The fax phone numbers for the organization where this application or proceeding is assigned are:

703-872-9306 for Official communications

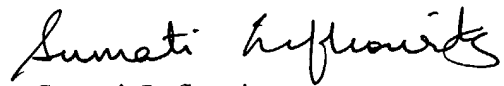
Application/Control Number: 09/802,417

Page 13

Art Unit: 2112

703-746-5661 for Non-Official/Draft communications

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.



Sumati Lefkowitz
Primary Examiner
Art Unit 2112

sl
August 23, 2004